

8GB 1G x 64-Bit DDR4-2666 CL19 1Rx8 260-Pin SODIMM (CBD26D4S9S8K1C-8)

Description

This document describes Kingston's 1G x 64-bit (8GB) DDR4-2666 CL19 SDRAM (Synchronous DRAM) 1Rx8, memory module, based on eight 1G x 8-bit SDRAMs. This 260-pin SODIMM uses gold contact fingers and requires +1.2V. The electrical and mechanical specifications are as follows:

Feature

- Power Supply: VDD = 1.2V
- VDDQ = 1.2V
- VPP = 2.5V
- VDDSPD = 2.20V to 3.60V
- Functionality and operations comply with the DDR4 SDRAM datasheet
- 16 internal banks (x4, x8): 4 groups of 4 banks each
- 8 internal banks (x16): 2 groups of 4 banks each
- Bank Grouping is applied, and CAS to CAS latency (tCCD_L, tCCD_S) for the banks in the same or different bank group accesses are available
- Data transfer rates: PC4-2666, PC4-2400, PC4-2133, PC4-1866, PC4-1600
- Bi-Directional Differential Data Strobe
- 8 bit pre-fetch
- Burst Length (BL) switch on-the-fly BL8 or BC4(Burst Chop)
- On-Die Termination (ODT)
- Per DRAM Addressability is supported
- Internal Vref DQ level generation is available
- Write CRC is supported at all speed grades
- CA parity (Command/Address Parity) mode is supported
- RoHS Compliant and Halogen-Free
- Gold Finger Plating Au 0.076um (Min)
- Operating Temperature 0° C to +85° C

*Products and specifications discussed herein are for evaluation and reference purposes only and are subject to change by without notice.
All information discussed herein is provided on an "as is" basis, without warranties of any kind.

SODIMM Pin Configuration (Front side/Back side)

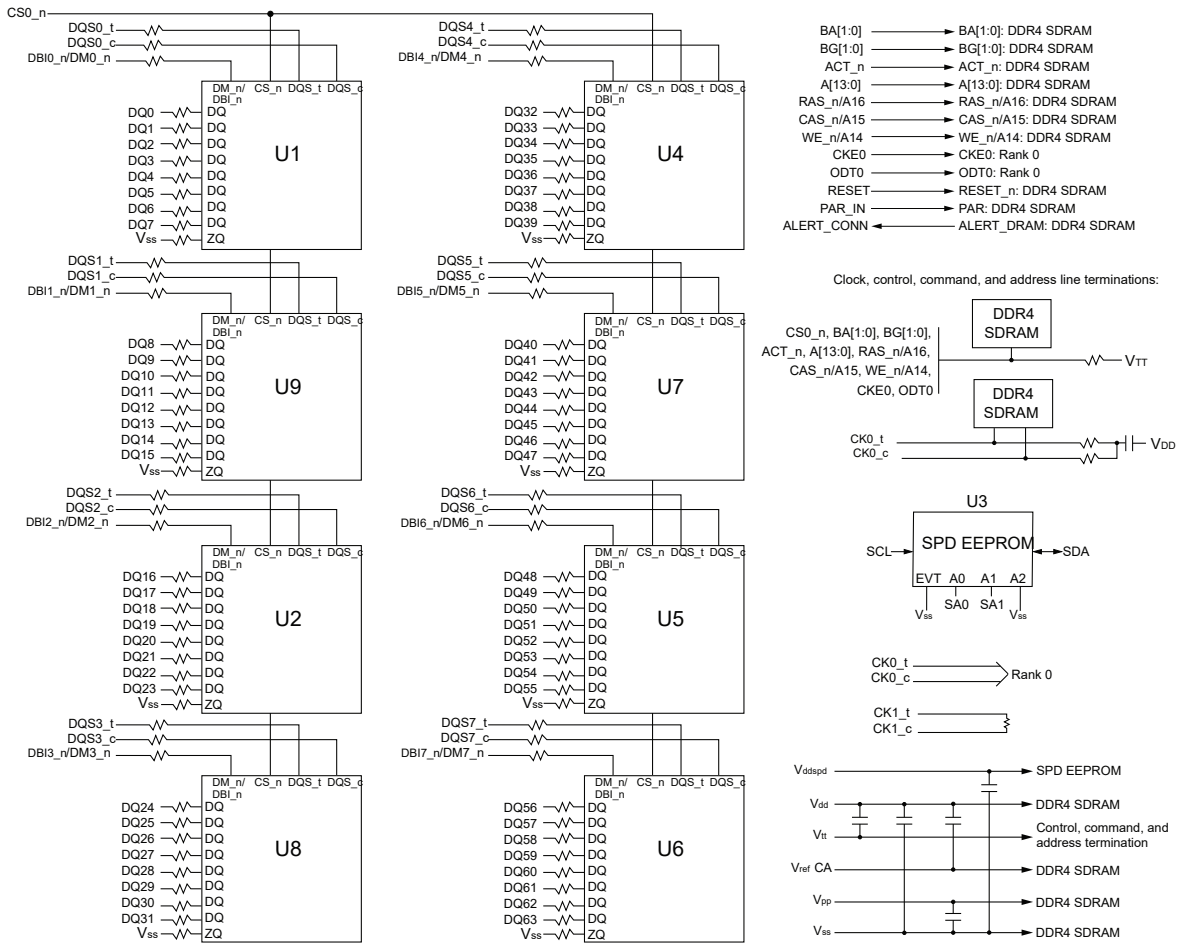
| Pin | Front | Pin | Back | Pin | Front | Pin | Back |
|-----|------------------|-----|------------------|-----|------------------|-----|------------------|
| 1 | VSS | 2 | VSS | 131 | A3 | 132 | A2 |
| 3 | DQ5 | 4 | DQ4 | 133 | A1 | 134 | EVENT_n |
| 5 | VSS | 6 | VSS | 135 | VDD | 136 | VDD |
| 7 | DQ1 | 8 | DQ0 | 137 | CK0_t | 138 | CK1_t |
| 9 | VSS | 10 | VSS | 139 | CK0_c | 140 | CK1_c |
| 11 | DQS0_c | 12 | DM0_n/DBI0_n, NC | 141 | VDD | 142 | VDD |
| 13 | DQS0_t | 14 | VSS | 143 | PARITY | 144 | A0 |
| 15 | VSS | 16 | DQ6 | KEY | | | |
| 17 | DQ7 | 18 | VSS | | | | |
| 19 | VSS | 20 | DQ2 | 145 | BA1 | 146 | A10/AP |
| 21 | DQ3 | 22 | VSS | 147 | VDD | 148 | VDD |
| 23 | VSS | 24 | DQ12 | 149 | CS0_n | 150 | BA0 |
| 25 | DQ13 | 26 | VSS | 151 | A14/WE_n | 152 | A16/RAS_n |
| 27 | VSS | 28 | DQ8 | 153 | VDD | 154 | VDD |
| 29 | DQ9 | 30 | VSS | 155 | ODT0 | 156 | A15/CAS_n |
| 31 | VSS | 32 | DQS1_c | 157 | CS1_n | 158 | A13 |
| 33 | DM1_n/DBI1_n, NC | 34 | DQS1_t | 159 | VDD | 160 | VDD |
| 35 | VSS | 36 | VSS | 161 | ODT1 | 162 | C0, CS2_n, NC |
| 37 | DQ15 | 38 | DQ14 | 163 | VDD | 164 | VREFCA |
| 39 | VSS | 40 | VSS | 165 | C1, CS3_n, NC | 166 | SA2 |
| 41 | DQ10 | 42 | DQ11 | 167 | VSS | 168 | VSS |
| 43 | VSS | 44 | VSS | 169 | DQ37 | 170 | DQ36 |
| 45 | DQ21 | 46 | DQ20 | 171 | VSS | 172 | VSS |
| 47 | VSS | 48 | VSS | 173 | DQ33 | 174 | DQ32 |
| 49 | DQ17 | 50 | DQ16 | 175 | VSS | 176 | VSS |
| 51 | VSS | 52 | VSS | 177 | DQS4_c | 178 | DM4_n/DBI4_n, NC |
| 53 | DQS2_c | 54 | DM2_n/DBI2_n, NC | 179 | DQS4_t | 180 | VSS |
| 55 | DQS2_t | 56 | VSS | 181 | VSS | 182 | DQ39 |
| 57 | VSS | 58 | DQ22 | 183 | DQ38 | 184 | VSS |
| 59 | DQ23 | 60 | VSS | 185 | VSS | 186 | DQ35 |
| 61 | VSS | 62 | DQ18 | 187 | DQ34 | 188 | VSS |
| 63 | DQ19 | 64 | VSS | 189 | VSS | 190 | DQ45 |
| 65 | VSS | 66 | DQ28 | 191 | DQ44 | 192 | VSS |
| 67 | DQ29 | 68 | VSS | 193 | VSS | 194 | DQ41 |
| 69 | VSS | 70 | DQ24 | 195 | DQ40 | 196 | VSS |
| 71 | DQ25 | 72 | VSS | 197 | VSS | 198 | DQS5_c |
| 73 | VSS | 74 | DQS3_c | 199 | DM5_n/DBI5_n, NC | 200 | DQS5_t |
| 75 | DM3_n/DBI3_n, NC | 76 | DQS3_t | 201 | VSS | 202 | VSS |

| Pin | Front | Pin | Back | Pin | Front | Pin | Back |
|-----|---------|-----|------------------|-----|------------------|-----|------------------|
| 77 | VSS | 78 | VSS | 203 | DQ46 | 204 | DQ47 |
| 79 | DQ30 | 80 | DQ31 | 205 | VSS | 206 | VSS |
| 81 | VSS | 82 | VSS | 207 | DQ42 | 208 | DQ43 |
| 83 | DQ26 | 84 | DQ27 | 209 | VSS | 210 | VSS |
| 85 | VSS | 86 | VSS | 211 | DQ52 | 212 | DQ53 |
| 87 | CB5, NC | 88 | CB4, NC | 213 | VSS | 214 | VSS |
| 89 | VSS | 90 | VSS | 215 | DQ49 | 216 | DQ48 |
| 91 | CB1, NC | 92 | CB0, NC | 217 | VSS | 218 | VSS |
| 93 | VSS | 94 | VSS | 219 | DQS6_c | 220 | DM6_n/DBI6_n, NC |
| 95 | DQS8_c | 96 | DM8_n/DBI8_n, NC | 221 | DQS6_t | 222 | VSS |
| 97 | DQS8_t | 98 | VSS | 223 | VSS | 224 | DQ54 |
| 99 | VSS | 100 | CB6, NC | 225 | DQ55 | 226 | VSS |
| 101 | CB2, NC | 102 | VSS | 227 | VSS | 228 | DQ50 |
| 103 | VSS | 104 | CB7, NC | 229 | DQ51 | 230 | VSS |
| 105 | CB3, NC | 106 | VSS | 231 | VSS | 232 | DQ60 |
| 107 | VSS | 108 | RESET_n | 233 | DQ61 | 234 | VSS |
| 109 | CKE0 | 110 | CKE1 | 235 | VSS | 236 | DQ57 |
| 111 | VDD | 112 | VDD | 237 | DQ56 | 238 | VSS |
| 113 | BG1 | 114 | ACT_n | 239 | VSS | 240 | DQS7_c |
| 115 | BG0 | 116 | ALERT_n | 241 | DM7_n/DBI7_n, NC | 242 | DQS7_t |
| 117 | VDD | 118 | VDD | 243 | VSS | 244 | VSS |
| 119 | A12 | 120 | A11 | 245 | DQ62 | 246 | DQ63 |
| 121 | A9 | 122 | A7 | 247 | VSS | 248 | VSS |
| 123 | VDD | 124 | VDD | 249 | DQ58 | 250 | DQ59 |
| 125 | A8 | 126 | A5 | 251 | VSS | 252 | VSS |
| 127 | A6 | 128 | A4 | 253 | SCL | 254 | SDA |
| 129 | VDD | 130 | VDD | 255 | VDDSPD | 256 | SA0 |
| | | | | 257 | VPP | 258 | VTT |
| | | | | 259 | VPP | 260 | SA1 |

Pin Descriptions

| Pin Name | Description | Pin Name | Description |
|--|---|--------------------|--|
| A0-A16 | SDRAM address bus | SCL | I ² C serial bus clock for SPD/TS |
| BA0, BA1 | SDRAM bank select | SDA | I ² C serial data line for SPD/TS |
| BG0, BG1 | SDRAM bank group select | SA0-SA2 | I ² C slave address select for SPD/TS |
| RAS _n ¹ | SDRAM row address strobe | PARITY | SDRAM parity input |
| CAS _n ² | SDRAM column address strobe | VDD | SDRAM I/O & core power supply |
| WE _n ³ | SDRAM write enable | VPP | SDRAM activating power supply |
| CS0 _n , CS1 _n , CS2 _n , CS3 _n | Rank Select Lines | C0, C1 | Chip ID lines for 3DS components |
| CKE0, CEK1 | SDRAM clock enable lines | VREFCA | SDRAM command/address reference supply |
| ODT0, ODT1 | SDRAM on-die termination control lines | VSS | Power supply return (ground) |
| ACT _n | SDRAM activate | VDDSPD | Serial SPD/TS positive power supply |
| DQ0-DQ63 | DIMM memory data bus | ALERT _n | SDRAM ALERT _n |
| CB0-CB7 | DIMM ECC check bits | | |
| DQS0 _t -DQS8 _t | SDRAM data strobe (positive line of differential pair) | RESET _n | Set SDRAMs to a Known State |
| DQS0 _c -DQS8 _c | SDRAM data strobe (negative line of differential pair) | EVENT _n | SPD signals a thermal event has occurred |
| DM0 _n -DM8 _n , DBI0 _n -DBI8 _n | SDRAM data masks/data bus inversion (x8-based x72 DIMMs) | VTT | Termination supply for the Address, Command and Control bus |
| CK0 _t , CK1 _t | SDRAM clock (positive line of differential pair) | NC | No connection |
| CK0 _c , CK1 _c | SDRAM clock (negative line of differential pair) | | |

Functional Block Diagram



Note: 1. The ZQ ball on each DDR4 component is connected to an external 240 Ω ±1% resistor that is tied to ground. It is used for the calibration of the component's ODT and output driver.

Absolute Maximum DC Ratings

Absolute Maximum DC Ratings

| Symbol | Parameter | Rating | Units | NOTE |
|------------------------------------|-------------------------------------|-------------|-------|------|
| VDD | Voltage on VDD pin relative to Vss | -0.3 ~ 1.5 | V | 1,3 |
| VDDQ | Voltage on VDDQ pin relative to Vss | -0.3 ~ 1.5 | V | 1,3 |
| VPP | Voltage on VPP pin relative to Vss | -0.3 ~ 3.0 | V | 4 |
| V _{IN} , V _{OUT} | Voltage on any pin relative to Vss | -0.3 ~ 1.5 | V | 1 |
| T _{STG} | Storage Temperature | -55 to +100 | °C | 1,2 |

NOTE :

- Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability
- Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JEDEC51-2 standard.
- VDD and VDDQ must be within 300 mV of each other at all times;and VREFCA must be not greater than 0.6 x VDDQ, When VDD and VDDQ are less than 500 mV; VREF may be equal to or less than 300 mV
- VPP must be equal or greater than VDD/VDDQ at all times

Recommended DC Operating Conditions

Recommended DC Operating Conditions

| Symbol | Parameter | Rating | | | Unit | NOTE |
|--------|------------------------------------|--------|------|------|------|-------|
| | | Min. | Typ. | Max. | | |
| VDD | Supply Voltage | 1.14 | 1.2 | 1.26 | V | 1,2,3 |
| VDDQ | Supply Voltage for Output | 1.14 | 1.2 | 1.26 | V | 1,2,3 |
| VPP | Supply Voltage for DRAM Activating | 2.375 | 2.5 | 2.75 | V | 3 |

NOTE:

- Under all conditions VDDQ must be less than or equal to VDD.
- VDDQ tracks with VDD. AC parameters are measured with VDD and VDDQ tied together.
- DC bandwidth is limited to 20MHz.

IDD Specifications

| Symbol | 2666 | Units |
|--------------------|------|-------|
| I _{DD0} | TBD | mA |
| I _{PP0} | TBD | mA |
| I _{DD1} | TBD | mA |
| I _{DD2N} | TBD | mA |
| I _{DD2NT} | TBD | mA |
| I _{DD2P} | TBD | mA |
| I _{DD2Q} | TBD | mA |
| I _{DD3N} | TBD | mA |
| I _{PP3N} | TBD | mA |
| I _{DD3P} | TBD | mA |
| I _{DD4R} | TBD | mA |
| I _{DD4W} | TBD | mA |
| I _{DD5R} | TBD | mA |
| I _{PP5R} | TBD | mA |
| I _{DD6N} | TBD | mA |
| I _{DD6E} | TBD | mA |
| I _{DD6R} | TBD | mA |
| I _{DD6A} | TBD | mA |
| I _{DD6A} | TBD | mA |
| I _{DD6A} | TBD | mA |
| I _{DD6A} | TBD | mA |
| I _{DD6A} | TBD | mA |
| I _{PP6X} | TBD | mA |
| I _{DD7} | TBD | mA |
| I _{PP7} | TBD | mA |
| I _{DD8} | TBD | mA |

Electrical Characteristics and AC timing

Refresh Parameters by Device Density

| Parameter | Symbol | 8Gb | Units | |
|---|--------|----------------------------------|-------|----|
| All Bank Refresh to active/refresh cmd time | tRFC1 | 350 | ns | |
| Average periodic refresh interval | tREFI1 | 0 °C ≤ T _{CASE} ≤ 85°C | 7.8 | μs |
| | | 85 °C < T _{CASE} ≤ 95°C | 3.9 | μs |

Speed Bins and CL, tRCD, tRP, tRC and tRAS for Corresponding Bin

| Speed | DDR4-2666 | Units | NOTE |
|-----------------------|-----------|-------|------|
| Bin (CL - tRCD - tRP) | 19-19-19 | | |
| Parameter | min | | |
| CL | 19 | tCK | |
| tRCD | 13.75 | ns | |
| tRP | 13.75 | ns | |
| tRAS | 32 | ns | |
| tRC | 45.75 | ns | |
| tRRDS | 3.0 | ns | |
| tFAW | 21 | ns | |

Timing Parameters

| Speed | | | | | | | | DDR4-2666 | | Units |
|---|-----------------------------|--|--|--|--|--|------------------|-----------|-----------------------|-----------------------|
| Parameter | Symbol | | | | | | MIN | MAX | | |
| Clock Timing | | | | | | | | | | |
| Minimum Clock Cycle Time (DLL off mode) | t _{CK} (DLL_OFF) | | | | | | 8 | 20 | ns | |
| Average Clock Period | t _{CK} (avg) | | | | | | 0.750 | <0.833 | ns | |
| Average high pulse width | t _{CH} (avg) | | | | | | 0.48 | 0.52 | t _{CK} (avg) | |
| Average low pulse width | t _{CL} (avg) | | | | | | 0.48 | 0.52 | t _{CK} (avg) | |
| Absolute Clock Period | t _{CK} (abs) | t _{CK} (avg)min + t _{JIT} (per)min_tot t _{CK} (avg)max + t _{JIT} (per)max_tot | | | | | | | | t _{CK} (avg) |
| Absolute clock HIGH pulse width | t _{CH} (abs) | | | | | | 0.45 | - | t _{CK} (avg) | |
| Absolute clock LOW pulse width | t _{CL} (abs) | | | | | | 0.45 | - | t _{CK} (avg) | |
| Clock Period Jitter- total | t _{JIT} (per)_tot | | | | | | -38 | 38 | ps | |
| Clock Period Jitter- deterministic | t _{JIT} (per)_dj | | | | | | -19 | 19 | ps | |
| Clock Period Jitter during DLL locking period | t _{JIT} (per, lck) | | | | | | -30 | 30 | ps | |
| Cycle to Cycle Period Jitter | t _{JIT} (cc)_total | | | | | | - | 75 | ps | |
| Cycle to Cycle Period Jitter during DLL locking period | t _{JIT} (cc, lck) | | | | | | - | 60 | ps | |
| Duty Cycle Jitter | t _{JIT} (duty) | | | | | | TBD | TBD | ps | |
| Cumulative error across 2 cycles | t _{ERR} (2per) | | | | | | -55 | 55 | ps | |
| Cumulative error across 3 cycles | t _{ERR} (3per) | | | | | | -66 | 66 | ps | |
| Cumulative error across 4 cycles | t _{ERR} (4per) | | | | | | -73 | 73 | ps | |
| Cumulative error across 5 cycles | t _{ERR} (5per) | | | | | | -78 | 78 | ps | |
| Cumulative error across 6 cycles | t _{ERR} (6per) | | | | | | -83 | 83 | ps | |
| Cumulative error across 7 cycles | t _{ERR} (7per) | | | | | | -87 | 87 | ps | |
| Cumulative error across 8 cycles | t _{ERR} (8per) | | | | | | -91 | 91 | ps | |
| Cumulative error across 9 cycles | t _{ERR} (9per) | | | | | | -94 | 94 | ps | |
| Cumulative error across 10 cycles | t _{ERR} (10per) | | | | | | -96 | 96 | ps | |
| Cumulative error across 11 cycles | t _{ERR} (11per) | | | | | | -99 | 99 | ps | |
| Cumulative error across 12 cycles | t _{ERR} (12per) | | | | | | -101 | 101 | ps | |
| Cumulative error across 13 cycles | t _{ERR} (13per) | | | | | | -103 | 103 | ps | |
| Cumulative error across 14 cycles | t _{ERR} (14per) | | | | | | -104 | 104 | ps | |
| Cumulative error across 15 cycles | t _{ERR} (15per) | | | | | | -106 | 106 | ps | |
| Cumulative error across 16 cycles | t _{ERR} (16per) | | | | | | -108 | 108 | ps | |
| Cumulative error across 17 cycles | t _{ERR} (17per) | | | | | | -110 | 110 | ps | |
| Cumulative error across 18 cycles | t _{ERR} (18per) | | | | | | -112 | 112 | ps | |
| Cumulative error across n = 13, 14 . . . 49, 50 cycles | t _{ERR} (nper) | t _{ERR} (nper)min = ((1 + 0.68ln(n)) * t _{JIT} (per)_total min) t _{ERR} (nper)max = ((1 + 0.68ln(n)) * t _{JIT} (per)_total max) | | | | | | | | ps |
| Command and Address setup time to CK_t, CK_c referenced to Vih(ac) / Vil(ac) levels | t _{IS} (base) | | | | | | TBD | - | ps | |
| Command and Address setup time to CK_t, CK_c referenced to Vref levels | t _{IS} (Vref) | | | | | | TBD | - | ps | |
| Command and Address hold time to CK_t, CK_c referenced to Vih(dc) / Vil(dc) levels | t _{IH} (base) | | | | | | TBD | - | ps | |
| Command and Address hold time to CK_t, CK_c referenced to Vref levels | t _{IH} (Vref) | | | | | | TBD | - | ps | |
| Control and Address Input pulse width for each input | t _{IPW} | | | | | | 385 | - | ps | |
| Command and Address Timing | | | | | | | | | | |
| CAS_n to CAS_n command delay for same bank group | t _{CCD_L} | | | | | | max(5 nCK, 5 ns) | - | nCK | |
| CAS_n to CAS_n command delay for different bank group | t _{CCD_S} | | | | | | 4 | - | nCK | |
| ACTIVATE to ACTIVATE Command delay to different bank group for 2KB page size | t _{RRD_S} (2K) | | | | | | Max(4nCK, 5.3ns) | - | nCK | |

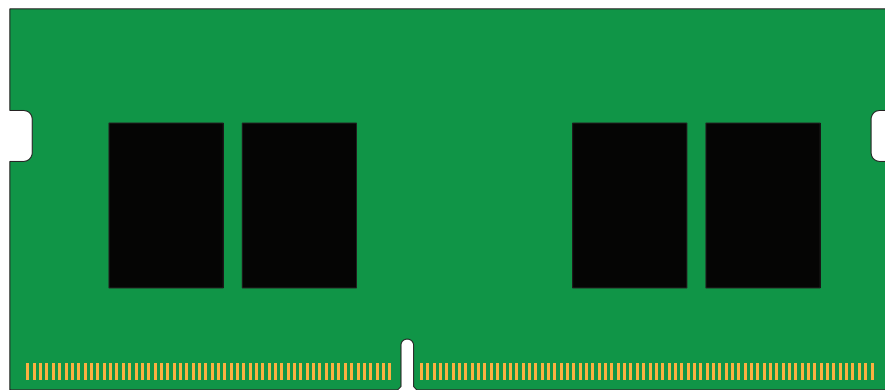
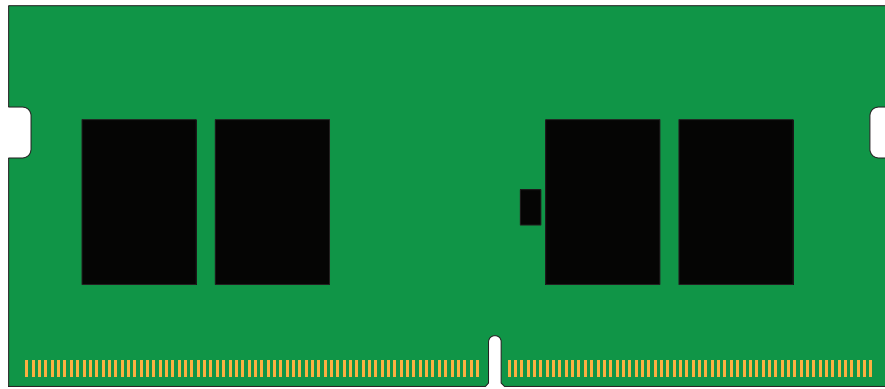
| Speed | | | | | | | | DDR4-2666 | | Units |
|---|----------------|--|--|--|--|--|--|---|------|-------------|
| Parameter | Symbol | | | | | | | MIN | MAX | |
| ACTIVATE to ACTIVATE Command delay to different bank group for 2KB page size | tRRD_S(1K) | | | | | | | Max(4nCK, 3ns) | - | nCK |
| ACTIVATE to ACTIVATE Command delay to different bank group for 1/2KB page size | tRRD_S(1/2K) | | | | | | | Max(4nCK, 3ns) | - | nCK |
| ACTIVATE to ACTIVATE Command delay to same bank group for 2KB page size | tRRD_L(2K) | | | | | | | Max(4nCK, 6.4ns) | - | nCK |
| ACTIVATE to ACTIVATE Command delay to same bank group for 1KB page size | tRRD_L(1K) | | | | | | | Max(4nCK, 4.9ns) | - | nCK |
| ACTIVATE to ACTIVATE Command delay to same bank group for 1/2KB page size | tRRD_L(1/2K) | | | | | | | Max(4nCK, 4.9ns) | - | nCK |
| Four activate window for 2KB page size | tFAW_2K | | | | | | | Max(28nCK, 30ns) | - | ns |
| Four activate window for 1KB page size | tFAW_1K | | | | | | | Max(20nCK, 21ns) | - | ns |
| Four activate window for 1/2KB page size | tFAW_1/2K | | | | | | | Max(16nCK, 12ns) | - | ns |
| Delay from start of internal write transaction to internal read command for different bank group | tWTR_S | | | | | | | max (2nCK, 2.5ns) | - | ns |
| Delay from start of internal write transaction to internal read command for same bank group | tWTR_L | | | | | | | max (4nCK, 7.5 ns) | - | ns |
| Internal READ Command to PRECHARGE Command delay | tRTP | | | | | | | max (4nCK, 7.5 ns) | - | ns |
| WRITE recovery time | tWR | | | | | | | 15 | - | ns |
| Write recovery time when CRC and DM are enabled | tWR_CRC_DM | | | | | | | tWR+max (5nCK, 3.7 5ns) | - | ns |
| delay from start of internal write transaction to internal read command for different bank group with both CRC and DM enabled | tWTR_S_C RC_DM | | | | | | | tWTR_S+ max (5nCK, 3.7 5ns) | - | ns |
| delay from start of internal write transaction to internal read command for same bank group with both CRC and DM enabled | tWTR_L_C RC_DM | | | | | | | tWTR_L+ max (5nCK, 3.7 5ns) | - | ns |
| DLL locking time | tDLLK | | | | | | | 854 | - | nCK |
| Mode Register Set command cycle time | tMRD | | | | | | | 8 | - | nCK |
| Mode Register Set command update delay | tMOD | | | | | | | max(24nCK, 15ns) | - | nCK |
| Multi-Purpose Register Recovery Time | tMPRR | | | | | | | 1 | - | nCK |
| Multi Purpose Register Write Recovery Time | tWR_MPR | | | | | | | tMOD (min) + AL + PL | - | nCK |
| Auto precharge write recovery + precharge time | tDAL(min) | | | | | | | Programmed WR + roundup (tRP / tCK(avg)) | | nCK |
| DQ0 or DQL0 driven to 0 set-up time to first DQS rising edge | tPDA_S | | | | | | | 0.5 | - | UI |
| DQ0 or DQL0 driven to 0 hold time from last DQS fall-ing edge | tPDA_H | | | | | | | 0.5 | - | UI |
| CS_n to Command Address Latency | | | | | | | | | | |
| CS_n to Command Address Latency | tCAL | | | | | | | max(3nCK, 3.748ns) | - | nCK |
| Mode Register Set cyce time in CAL mode | tMRD_tCAL | | | | | | | tMOD+ tCAL | - | nCK |
| Mode Register Set update delay in CAL mode | tMOD_tCAL | | | | | | | tMOD+ tCAL | - | nCK |
| DRAM Data Timing | | | | | | | | | | |
| DQS_t, DQS_c to DQ skew, per group, per access | tDQSQ | | | | | | | - | 0.18 | tCK(avg)/ 2 |
| DQ output hold per group, per access from DQS_t, DQS_c | tQH | | | | | | | 0.74 | - | tCK(avg)/ 2 |
| Data Valid Window per device: (tQH - tDQSQ) of each UI on a given DRAM | tDVWd | | | | | | | TBD | - | UI |
| Data Valid Window , per pin per UI : (tQH - tDQSQ) each UI on a pin of a given DRAM | tDVWp | | | | | | | 0.72 | - | UI |
| DQ low impedance time from CK_t, CK_c | tLZ(DQ) | | | | | | | -310 | 170 | ps |
| DQ high impedance time from CK_t, CK_c | tHZ(DQ) | | | | | | | - | 170 | ps |
| Data Strobe Timing | | | | | | | | | | |

| Speed | | | | | | | | DDR4-2666 | | Units |
|---|------------------|--|--|--|--|--|----------------------------|-----------|-----|-------|
| Parameter | Symbol | | | | | | MIN | MAX | | |
| DQS_t, DQS_c differential READ Preamble | tRPRE | | | | | | 0.9 | | tCK | |
| | tRPRE2 | | | | | | 1.8 | | tCK | |
| DQS_t, DQS_c differential READ Postamble | tRPST | | | | | | 0.33 | | tCK | |
| DQS_t, DQS_c differential output high time | tQSH | | | | | | 0.4 | - | tCK | |
| DQS_t, DQS_c differential output low time | tQSL | | | | | | 0.4 | - | tCK | |
| DQS_t, DQS_c differential WRITE Preamble | tWPRE | | | | | | 0.9 | - | tCK | |
| | tWPRE2 | | | | | | 1.8 | - | tCK | |
| DQS_t, DQS_c differential WRITE Postamble | tWPST | | | | | | 0.33 | - | tCK | |
| DQS_t and DQS_c low-impedance time (Referenced from RL-1) | tLZ(DQS) | | | | | | -310 | 170 | ps | |
| DQS_t and DQS_c high-impedance time (Referenced from RL+BL/2) | tHZ(DQS) | | | | | | - | 170 | ps | |
| DQS_t, DQS_c differential input low pulse width | tDQSL | | | | | | 0.46 | 0.54 | tCK | |
| DQS_t, DQS_c differential input high pulse width | tDQSH | | | | | | 0.46 | 0.54 | tCK | |
| DQS_t, DQS_c rising edge to CK_t, CK_c rising edge (1 clock preamble) | tDQSS | | | | | | -0.27 | 0.27 | tCK | |
| DQS_t, DQS_c falling edge setup time to CK_t, CK_c rising edge | tDSS | | | | | | 0.18 | - | tCK | |
| DQS_t, DQS_c falling edge hold time from CK_t, CK_c rising edge | tDSH | | | | | | 0.18 | - | tCK | |
| DQS_t, DQS_c rising edge output timing locatino from rising CK_t, CK_c with DLL On mode | tDQSCK (DLL On) | | | | | | -170 | 170 | ps | |
| DQS_t, DQS_c rising edge output variance window per DRAM | tDQSCKI (DLL On) | | | | | | | 270 | ps | |
| MPSM Timing | | | | | | | | | | |
| Command path disable delay upon MPSM entry | tMPED | | | | | | TBD | - | | |
| Valid clock requirement after MPSM entry | tCKMPE | | | | | | TBD | - | | |
| Valid clock requirement before MPSM exit | tCKMPX | | | | | | TBD | - | | |
| Exit MPSM to commands not requiring a locked DLL | tXMP | | | | | | TBD | - | | |
| Exit MPSM to commands requiring a locked DLL | tXMPDLL | | | | | | TBD | - | | |
| CS setup time to CKE | tMPX_S | | | | | | TBD | - | | |
| Calibration Timing | | | | | | | | | | |
| Power-up and RESET calibration time | tZQinit | | | | | | 1024 | - | nCK | |
| Normal operation Full calibration time | tZQoper | | | | | | 512 | - | nCK | |
| Normal operation Short calibration time | tZQCS | | | | | | 128 | - | nCK | |
| Reset/Self Refresh Timing | | | | | | | | | | |
| Exit Reset from CKE HIGH to a valid command | tXPR | | | | | | max (5nCK, tRFC(min)+10ns) | - | nCK | |
| Exit Self Refresh to commands not requiring a locked DLL | tXS | | | | | | tRFC(min)+10ns | - | nCK | |
| SRX to commands not requiring a locked DLL in Self Refresh ABORT | tX-S_ABORT(min) | | | | | | tRFC4(min)+10ns | - | nCK | |
| Exit Self Refresh to ZQCL, ZQCS and MRS (CL, CWL, WR, RTP and Gear Down) | tXS_FAST (min) | | | | | | tRFC4(min)+10ns | - | nCK | |
| Exit Self Refresh to commands requiring a locked DLL | tXSDLL | | | | | | tDLLK(min) | - | nCK | |
| Minimum CKE low width for Self refresh entry to exit timing | tCKESR | | | | | | tCKE(min)+1nCK | - | nCK | |

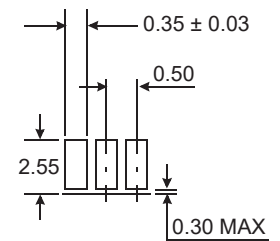
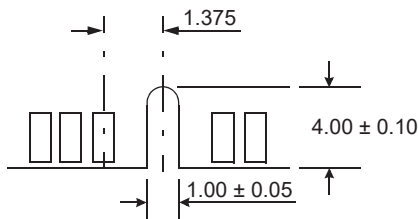
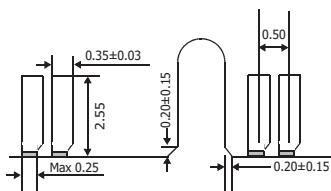
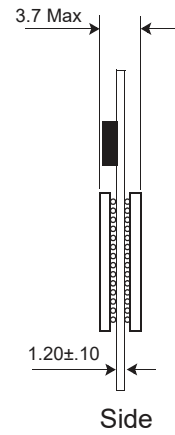
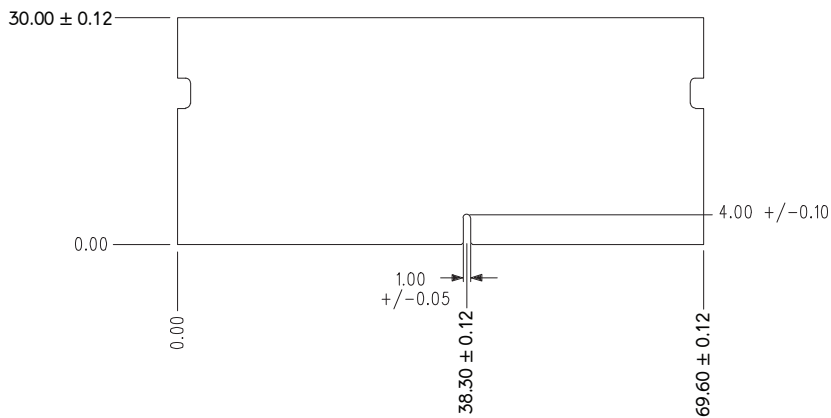
| Speed | | | | | | | | DDR4-2666 | | Units |
|--|---------------|--|--|--|--|--|----------------------|-----------|----------|-------|
| Parameter | Symbol | | | | | | MIN | MAX | | |
| Minimum CKE low width for Self refresh entry to exit timing with CA Parity enabled | tCKESR_PAR | | | | | | tCKE(min) + 1nCK+PL | - | nCK | |
| Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down Entry (PDE) | tCKSRE | | | | | | max (5nCK, 10 ns) | - | nCK | |
| Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down when CA Parity is enabled | tCKSRE_PAR | | | | | | max (5nCK, 10 ns)+PL | - | nCK | |
| Valid Clock Requirement before Self Refresh Exit (SRX) or Power-Down Exit (PDX) or Reset Exit | tCKSRX | | | | | | max (5nCK, 10 ns) | - | nCK | |
| Power Down Timing | | | | | | | | | | |
| Exit Power Down with DLL on to any valid command; Exit Precharge Power Down with DLL frozen to commands not requiring a locked DLL | tXP | | | | | | max (4nCK, 6ns) | - | nCK | |
| CKE minimum pulse width | tCKE | | | | | | max (3nCK, 5ns) | - | nCK | |
| Command pass disable delay | tCPDED | | | | | | 4 | - | nCK | |
| Power Down Entry to Exit Timing | tPD | | | | | | tCKE(min) | 9*tREFI | nCK | |
| Timing of ACT command to Power Down entry | tACTPDEN | | | | | | 2 | - | nCK | |
| Timing of PRE or PREA command to Power Down entry | tPRPDEN | | | | | | 2 | - | nCK | |
| Timing of RD/RDA command to Power Down entry | tRDPDEN | | | | | | RL+4+1 | - | nCK | |
| Timing of WR command to Power Down entry (BL8OTF, BL8MRS, BC4OTF) | tWRPDEN | | | | | | WL+4+(tWR/tCK(avg)) | - | nCK | |
| Timing of WRA command to Power Down entry (BL8OTF, BL8MRS, BC4OTF) | tWRAPDEN | | | | | | WL+4+W R+1 | - | nCK | |
| Timing of WR command to Power Down entry (BC4MRS) | tWRP-BC4DEN | | | | | | WL+2+(tWR/tCK(avg)) | - | nCK | |
| Timing of WRA command to Power Down entry (BC4MRS) | tWRAP-BC4DEN | | | | | | WL+2+W R+1 | - | nCK | |
| Timing of REF command to Power Down entry | tREFPDEN | | | | | | 2 | - | nCK | |
| Timing of MRS command to Power Down entry | tMRSPDEN | | | | | | tMOD(min) | - | nCK | |
| PDA Timing | | | | | | | | | | |
| Mode Register Set command cycle time in PDA mode | tMRD_PDA | | | | | | max(16nCK, 10ns) | - | nCK | |
| Mode Register Set command update delay in PDA mode | tMOD_PDA | | | | | | tMOD | | nCK | |
| ODT Timing | | | | | | | | | | |
| Asynchronous RTT turn-on delay (Power-Down with DLL frozen) | tAONAS | | | | | | 1.0 | 9.0 | ns | |
| Asynchronous RTT turn-off delay (Power-Down with DLL frozen) | tAOFAS | | | | | | 1.0 | 9.0 | ns | |
| RTT dynamic change skew | tADC | | | | | | 0.3 | 0.7 | tCK(avg) | |
| Write Leveling Timing | | | | | | | | | | |
| First DQS_t/DQS_n rising edge after write leveling mode is programmed | tWLMRD | | | | | | 40 | - | nCK | |
| DQS_t/DQS_n delay after write leveling mode is programmed | tWLDQSEN | | | | | | 25 | - | nCK | |
| Write leveling setup time from rising CK_t, CK_c crossing to rising DQS_t/DQS_n crossing | tWLS | | | | | | 0.13 | - | tCK(avg) | |
| Write leveling hold time from rising DQS_t/DQS_n crossing to rising CK_t, CK_c crossing | tWLH | | | | | | 0.13 | - | tCK(avg) | |
| Write leveling output delay | tWLO | | | | | | 0 | 9.5 | ns | |
| Write leveling output error | tWLOE | | | | | | 0 | 2 | ns | |
| CA Parity Timing | | | | | | | | | | |
| Commands not guaranteed to be executed during this time | tPAR_UNKNOWN | | | | | | - | PL | nCK | |
| Delay from errant command to ALERT_n assertion | tPAR_ALERT_ON | | | | | | - | PL+6ns | nCK | |

| Speed | | | | | | | | DDR4-2666 | | Units |
|---|----------------|--|--|--|--|--|--|-----------|-----|-------|
| Parameter | Symbol | | | | | | | MIN | MAX | |
| Pulse width of ALERT_n signal when asserted | tPAR_ALERT_PW | | | | | | | 80 | 160 | nCK |
| Time from when Alert is asserted till controller must start providing DES commands in Persistent CA parity mode | tPAR_ALERT_RSP | | | | | | | | 71 | nCK |
| Parity Latency | PL | | | | | | | 5 | | nCK |
| CRC Error Reporting | | | | | | | | | | |
| CRC error to ALERT_n latency | tCRC_ALERT | | | | | | | 3 | 13 | ns |
| CRC ALERT_n pulse width | CRC_ALERT_PW | | | | | | | 6 | 10 | nCK |
| Geardown timing | | | | | | | | | | |
| Exit RESET from CKE HIGH to a valid MRS geardown (T2/Reset) | tXPR_GEAR | | | | | | | TBD | | |
| CKE High Assert to Gear Down Enable time(T2/CKE) | tXS_GEAR | | | | | | | TBD | | |
| MRS command to Sync pulse time(T3) | tSYNC_GEAR | | | | | | | TBD | - | |
| Sync pulse to First valid command(T4) | tCMD_GEAR | | | | | | | TBD | | |
| Geardown setup time | tGEAR_setup | | | | | | | 2 | - | nCK |
| Geardown hold time | tGEAR_hold | | | | | | | 2 | - | nCK |
| tREFI | | | | | | | | | | |
| tRFC1 (min) | 2Gb | | | | | | | 160 | - | ns |
| | 4Gb | | | | | | | 260 | - | ns |
| | 8Gb | | | | | | | 350 | - | ns |
| | 16Gb | | | | | | | TBD | - | ns |
| tRFC2 (min) | 2Gb | | | | | | | 110 | - | ns |
| | 4Gb | | | | | | | 160 | - | ns |
| | 8Gb | | | | | | | 260 | - | ns |
| | 16Gb | | | | | | | TBD | - | ns |
| tRFC4 (min) | 2Gb | | | | | | | 90 | - | ns |
| | 4Gb | | | | | | | 110 | - | ns |
| | 8Gb | | | | | | | 160 | - | ns |
| | 16Gb | | | | | | | TBD | - | ns |

PACKAGE DIMENSIONS



All measurements are in millimeters.
(Tolerances on all dimensions are ± 0.12 unless otherwise specified)



SPD Content

| Byte | Function Described | Function Supported | Hex Value |
|-------|--|---------------------------------|-----------|
| 0 | Number of Bytes Used / Number of Bytes in SPD Device / CRC Coverage | 512Bytes Total, 384Bytes Used | 23 |
| 1 | SPD Revision | Ver 1.1 | 11 |
| 2 | Key Byte / DRAM Device Type | DDR4 SDRAM | 0C |
| 3 | Key Byte / Module Type | SODIMM | 03 |
| 4 | SDRAM Density and Banks | 8Gb, 4BG&4Banks | 85 |
| 5 | SDRAM Addressing | Row bits 16, Column bits 10 | 21 |
| 6 | SDRAM Device Type | Monolithic Device | 00 |
| 7 | SDRAM Optional Features | Unlimited MAC | 08 |
| 8 | SDRAM Thermal and Refresh Option | Reserved | 00 |
| 9 | Other SDRAM Optional Features | PPR supported | 60 |
| 10 | Reserved | Reserved | 00 |
| 11 | Module Nominal Voltage, VDD | 1.2V | 03 |
| 12 | Module Organization | 1Rx8 | 01 |
| 13 | Module Memory Bus Width | LP/x64 | 03 |
| 14 | Module Thermal Sensor | Thermal sensor not incorporated | 00 |
| 15-16 | Reserved | Reserved | 00 |
| 17 | Timebases | MTB 125ps, FTB 1ps | 00 |
| 18 | SDRAM Minimum Cycle Time(tckavg min) | 0.75ns | 06 |
| 19 | SDRAM Minimum Cycle Time(tckavg max) | 1.6ns | 0D |
| 20 | Cas Latency Supported, First Byte | 14, 13, 12, 11, 10 | F8 |
| 21 | Cas Latency Supported, Second Byte | 20, 19, 18, 17, 16, 15 | 3F |
| 22 | Cas Latency Supported, Third Byte | | 00 |
| 23 | Cas Latency Supported, Fourth Byte | | 00 |
| 24 | Minimum Cas Latency Time (tAamin) | 13.75ns | 6E |
| 25 | Minimum RAS to CAS Delay Time(tRCD min) | 13.75ns | 6E |
| 26 | Minimum Raw Precharge Delay Time(tRP min) | 13.75ns | 6E |
| 27 | Upper Nibbles for tRASmin and tRCmin | 32ns / 45.75ns | 11 |
| 28 | Minimum Active to Precharge Delay Time (tRASmin), Least Significant Byte | 32ns | 00 |
| 29 | Minimum Active to Active/Refresh Delay Time (tRCmin), Least Significant Byte | 45.75ns | 6E |
| 30 | Minimum Refresh Recovery Delay Time (tRFC1min), LSB | 350ns | F0 |
| 31 | Minimum Refresh Recovery Delay Time (tRFC1min), MSB | 350ns | 0A |
| 32 | Minimum Refresh Recovery Delay Time (tRFC2min), LSB | 260ns | 20 |
| 33 | Minimum Refresh Recovery Delay Time (tRFC2min), MSB | 260ns | 08 |
| 34 | Minimum Refresh Recovery Delay Time (tRFC4min), LSB | 160ns | 00 |
| 35 | Minimum Refresh Recovery Delay Time (tRFC4min), MSB | 160ns | 05 |
| 36 | Minimum Four Active Window Time (tFAWmin), Most Significant Nibble | 21ns | 00 |
| 37 | Minimum Four Activate Window Time (tFAWmin), Least Significant Byte | 21ns | A8 |
| 38 | Minimum Active to Active Delay Time (tRRD_smin), different Bank Group | 3.0ns | 18 |
| 39 | Minimum Active to Active Delay Time (tRRD_Lmin), Same Bank Group | 4.9ns | 28 |
| 40 | Minimum CAS to CAS Delay Time(tCCD_Lmin), same bank group | 5.0ns | 28 |

SPD Content(cont)

| Byte | Function Described | Function Supported | Hex Value |
|--------|--|--------------------|-----------|
| 41 | Upper Nibble for tWRmin | 15ns | 00 |
| 42 | Minimum Write Recovery Time(tWRmin) | 15ns | 78 |
| 43 | Upper Nibbles for tWTRmin | 7.5ns / 2.5ns | 00 |
| 44 | Minimum Write to Read Time(tWTR_smin), different bank group | 2.5ns | 14 |
| 45 | Minimum Write to Read Time(tWTR_Lmin), same bank group | 7.5ns | 3C |
| 46~59 | Reserved | Reserved | 00 |
| 60 | Connector to SDRAM Bit Mapping | | 2C |
| 61 | Connector to SDRAM Bit Mapping | | 16 |
| 62 | Connector to SDRAM Bit Mapping | | 2D |
| 63 | Connector to SDRAM Bit Mapping | | 04 |
| 64 | Connector to SDRAM Bit Mapping | | 2C |
| 65 | Connector to SDRAM Bit Mapping | | 16 |
| 66 | Connector to SDRAM Bit Mapping | | 2D |
| 67 | Connector to SDRAM Bit Mapping | | 03 |
| 68 | Connector to SDRAM Bit Mapping | | 00 |
| 69 | Connector to SDRAM Bit Mapping | | 00 |
| 70 | Connector to SDRAM Bit Mapping | | 2B |
| 71 | Connector to SDRAM Bit Mapping | | 15 |
| 72 | Connector to SDRAM Bit Mapping | | 04 |
| 73 | Connector to SDRAM Bit Mapping | | 2D |
| 74 | Connector to SDRAM Bit Mapping | | 2C |
| 75 | Connector to SDRAM Bit Mapping | | 0C |
| 76 | Connector to SDRAM Bit Mapping | | 2D |
| 77 | Connector to SDRAM Bit Mapping | | 03 |
| 78~116 | Reserved | Reserved | 00 |
| 117 | Fine Offset for Minimum CAS to CAS Delay Time(tCCD_Lmin), same bank group | 5.0ns | 00 |
| 118 | Fine Offset for Minimum Activate to Acticate Delay Time(tRRD_L_min), Same Bank Group | 4.90ns | 9C |
| 119 | Fine Offset for Minimum Activate to Acticate Delay Time(tRRD_Smin), Different Bank Group | 3.00ns | 00 |
| 120 | Fine Offset for Minimum Activate to Acticate/Refresh Delay Time(tRCmin) | 45.75ns | 00 |
| 121 | Fine Offset for Minimum Row Precharge Delay Time(tRPmin) | 13.75ns | 00 |
| 122 | Fine Offset for Minimum RAS to CAS Delay Time(tRCD_min) | 13.75ns | 00 |
| 123 | Fine Offset for Minimum CAS Latency Delay Time(tAA_min) | 13.75ns | 00 |
| 124 | Fine Offset for DRAM Maximum Cycle Time(tCKAVG_max) | 1.6ns | E7 |
| 125 | Fine Offset for DRAM Minimum Cycle Time(tCKAVG_min) | 0.75ns | 00 |
| 126 | Cyclical Redundancy Code | - | 77 |
| 127 | Cyclical Redundancy Code | - | B3 |
| 128 | Raw Card Extension, Module Nominal Height | 30.00mm | 0F |
| 129 | Module Maximum Thickness | | 11 |
| 130 | Reference Raw Card Used | A2 | 40 |
| 131 | Address Mapping from Edge Connector to DRAM | Standard | 00 |
| 132 | Reserved | Reserved | 00 |
| 133 | Reserved | Reserved | 00 |
| 134 | Reserved | Reserved | 00 |
| 135 | Reserved | Reserved | 00 |
| 136 | Reserved | Reserved | 00 |
| 137 | Reserved | Reserved | 00 |

SPD Content(cont)

| Byte | Function Described | Function Supported | Hex Value |
|---------|---|--------------------|-----------|
| 138 | Reserved | Reserved | 00 |
| 139~253 | Reserved | Reserved | 00 |
| 254 | Cyclical Redundancy Code | - | 30 |
| 255 | Cyclical Redundancy Code | - | 4C |
| 256~319 | Reserved | Reserved | 00 |
| 320 | Module Manufacturer's ID Code, Least Significant Byte | Kingston | 01 |
| 321 | Module Manufacturer's ID Code, Most Significant Byte | Kingston | 98 |
| 322 | Module Manufacturing Location | | 00 |
| 323 | Module Manufacturing Date | Variable | 00 |
| 324 | Module Manufacturing Date | Variable | 00 |
| 325 | Module Serial Number | - | 00 |
| 326 | Module Serial Number | - | 00 |
| 327 | Module Serial Number | - | 00 |
| 328 | Module Serial Number | - | 00 |
| 329 | Module Part Number | C | 43 |
| 330 | Module Part Number | B | 42 |
| 331 | Module Part Number | D | 44 |
| 332 | Module Part Number | 2 | 32 |
| 333 | Module Part Number | 6 | 36 |
| 334 | Module Part Number | D | 44 |
| 335 | Module Part Number | 4 | 34 |
| 336 | Module Part Number | S | 53 |
| 337 | Module Part Number | 9 | 39 |
| 338 | Module Part Number | S | 53 |
| 339 | Module Part Number | 8 | 38 |
| 340 | Module Part Number | K | 4B |
| 341 | Module Part Number | 1 | 31 |
| 342 | Module Part Number | C | 43 |
| 343 | Module Part Number | - | 2D |
| 344 | Module Part Number | 8 | 38 |
| 345 | Module Part Number | Blank | 20 |
| 346 | Module Part Number | Blank | 20 |
| 347 | Module Part Number | Blank | 20 |
| 348 | Module Part Number | Blank | 20 |
| 349 | Module Revision Code | | 00 |
| 350 | DRAM Manufacturer's ID Code, Least Significant Byte | Kingston | 01 |
| 351 | DRAM Manufacturer's ID Code, Most Significant Byte | Kingston | 98 |
| 352 | DRAM Stepping | C-die | 43 |
| 353~381 | Module Manufacturer's Specific Data | Reserved | 00 |
| 382~383 | Reserved | Reserved | 00 |
| 384~511 | End User Programmable | Reserved | 00 |